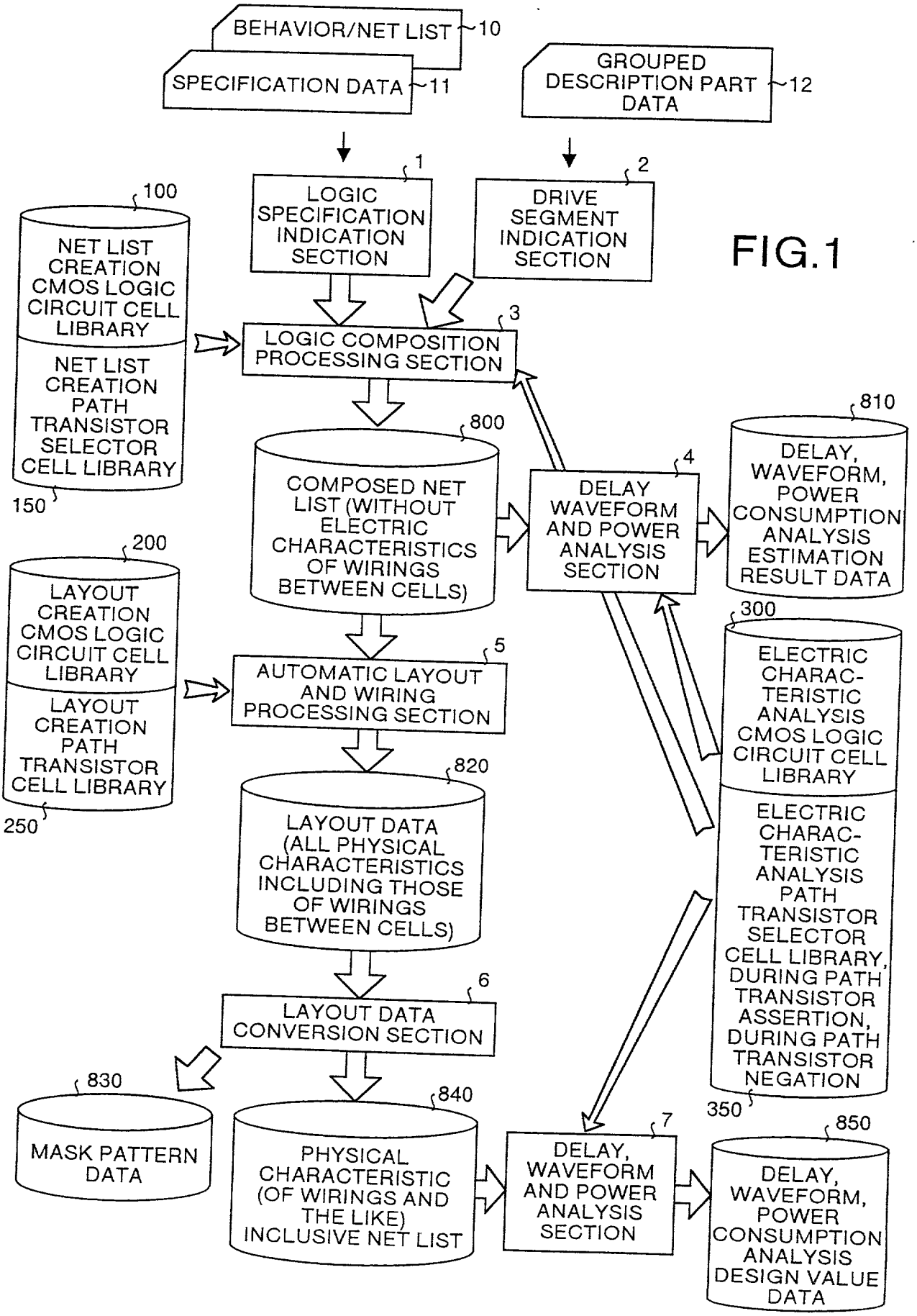


FIG.1

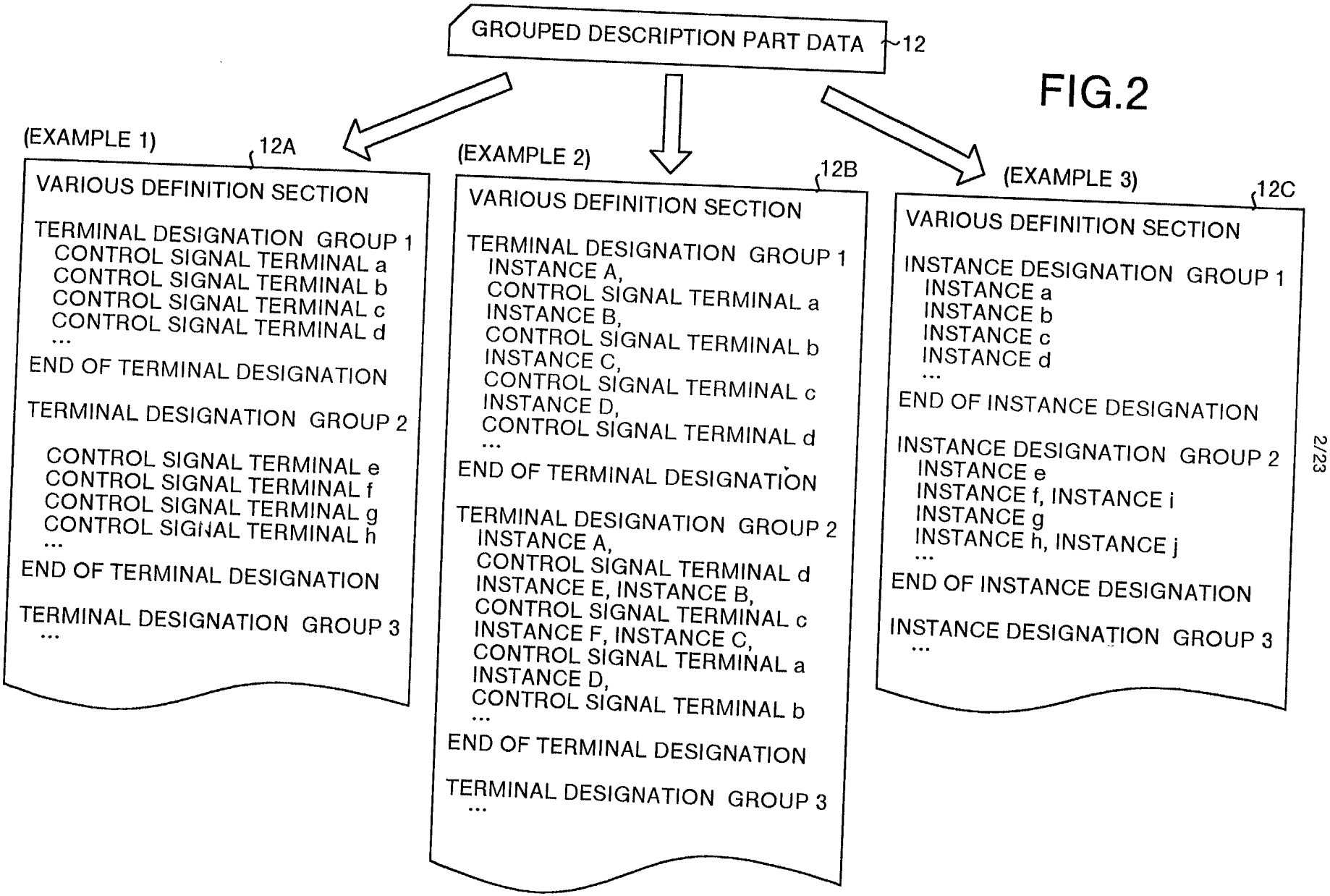


FIG.2

FIG.3

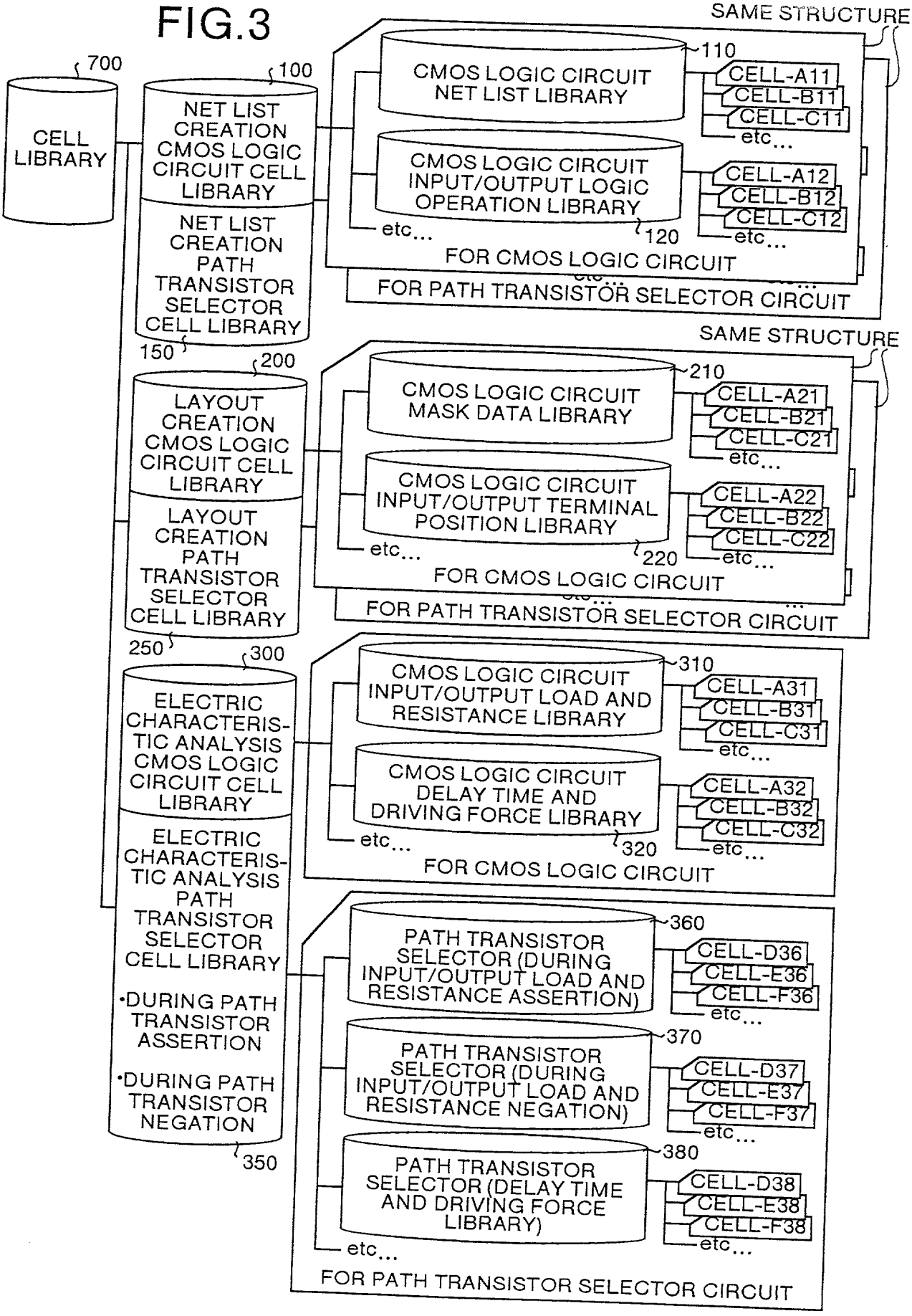


FIG.4

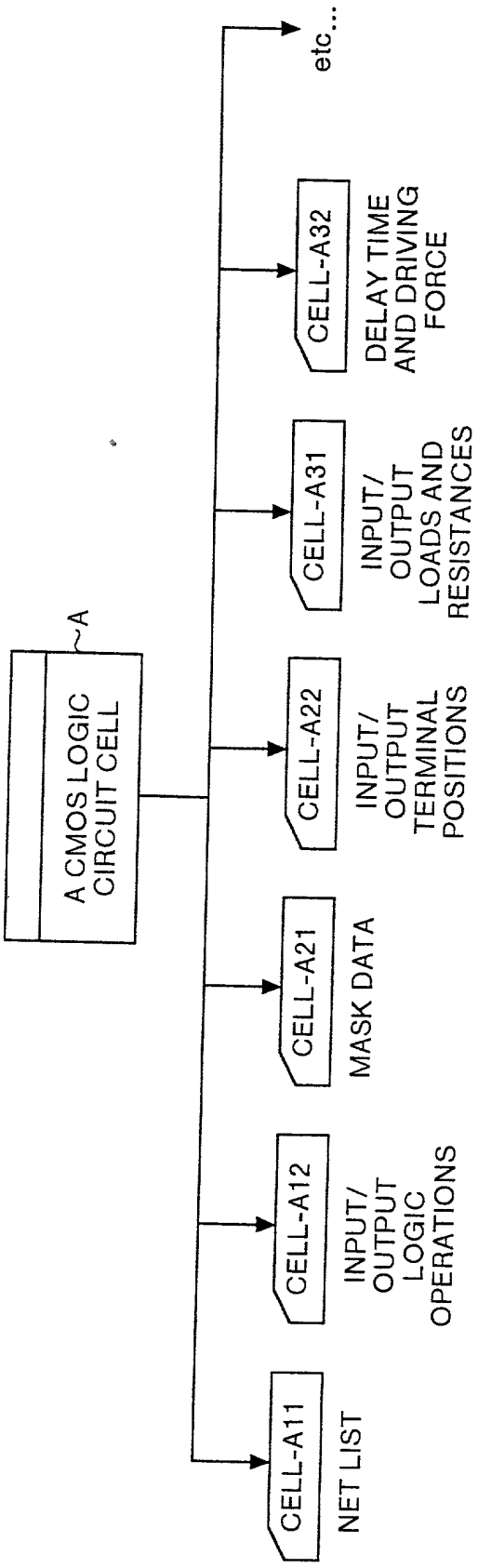

A CMOS LOGIC CIRCUIT CELL
A
CELL-A11
NET LIST
CELL-A12
INPUT/ OUTPUT LOGIC OPERATIONS
CELL-A21
MASK DATA
CELL-A22
INPUT/ OUTPUT TERMINAL POSITIONS
CELL-A31
INPUT/ OUTPUT LOADS AND RESISTANCES
CELL-A32
DELAY TIME AND DRIVING FORCE
etc...

FIG.5

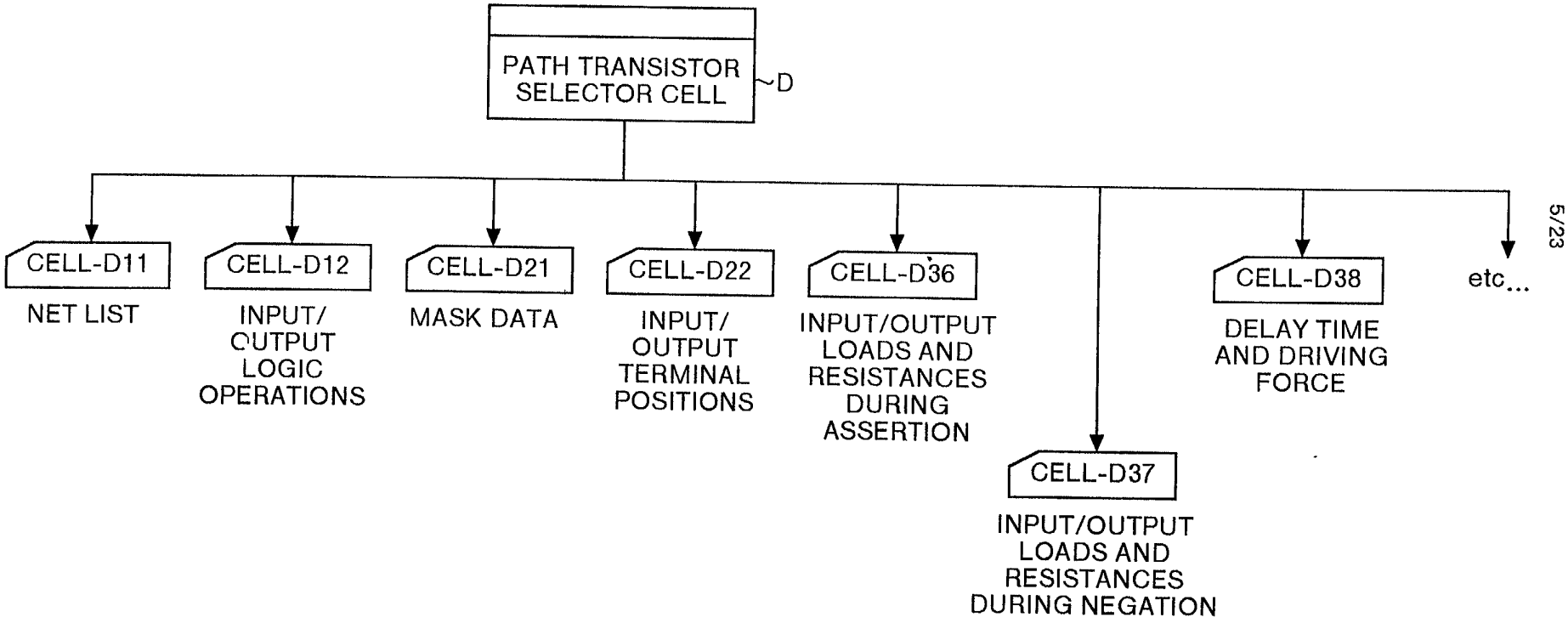

PATH TRANSISTOR SELECTOR CELL
D
CELL-D11
NET LIST
CELL-D12
INPUT/ OUTPUT LOGIC OPERATIONS
CELL-D21
MASK DATA
CELL-D22
INPUT/ OUTPUT TERMINAL POSITIONS
CELL-D36
INPUT/OUTPUT LOADS AND RESISTANCES DURING ASSERTION
CELL-D37
INPUT/OUTPUT LOADS AND RESISTANCES DURING NEGATION
CELL-D38
DELAY TIME AND DRIVING FORCE
etc...

FIG.6A

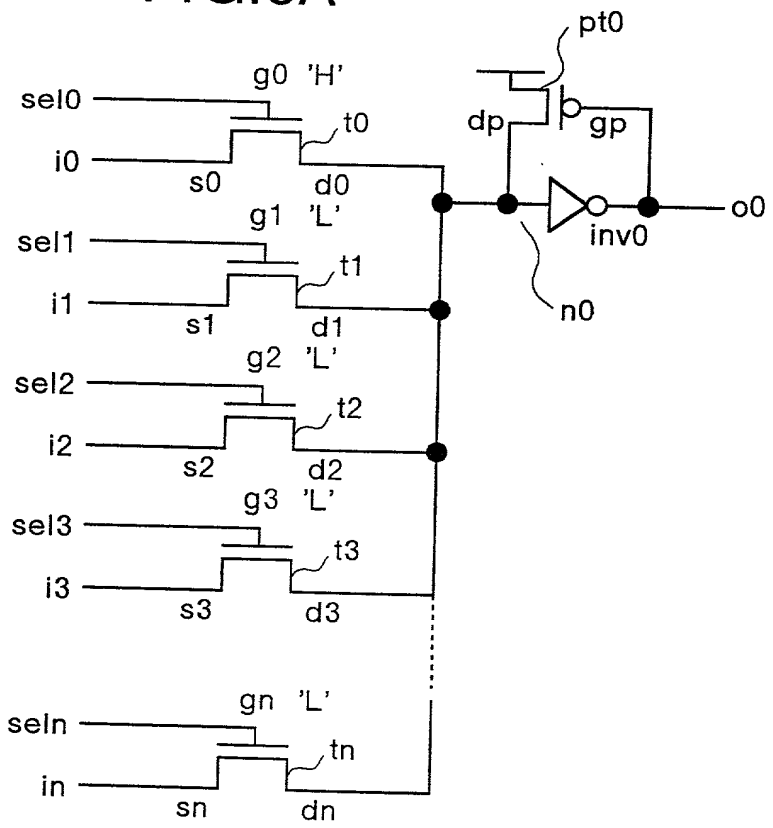

pt0
g0 'H'
sel0
t0
dp
gp
i0
s0
d0
o0
g1 'L'
inv0
sel1
t1
i1
s1
d1
n0
g2 'L'
sel2
t2
i2
s2
d2
g3 'L'
sel3
t3
i3
s3
d3
gn 'L'
seln
tn
in
sn
dn

FIG.6B

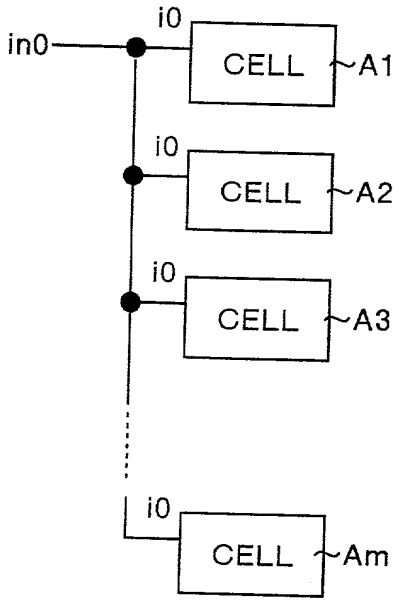

in0
i0
CELL
A1
i0
CELL
A2
i0
CELL
A3
i0
CELL
Am

FIG.7

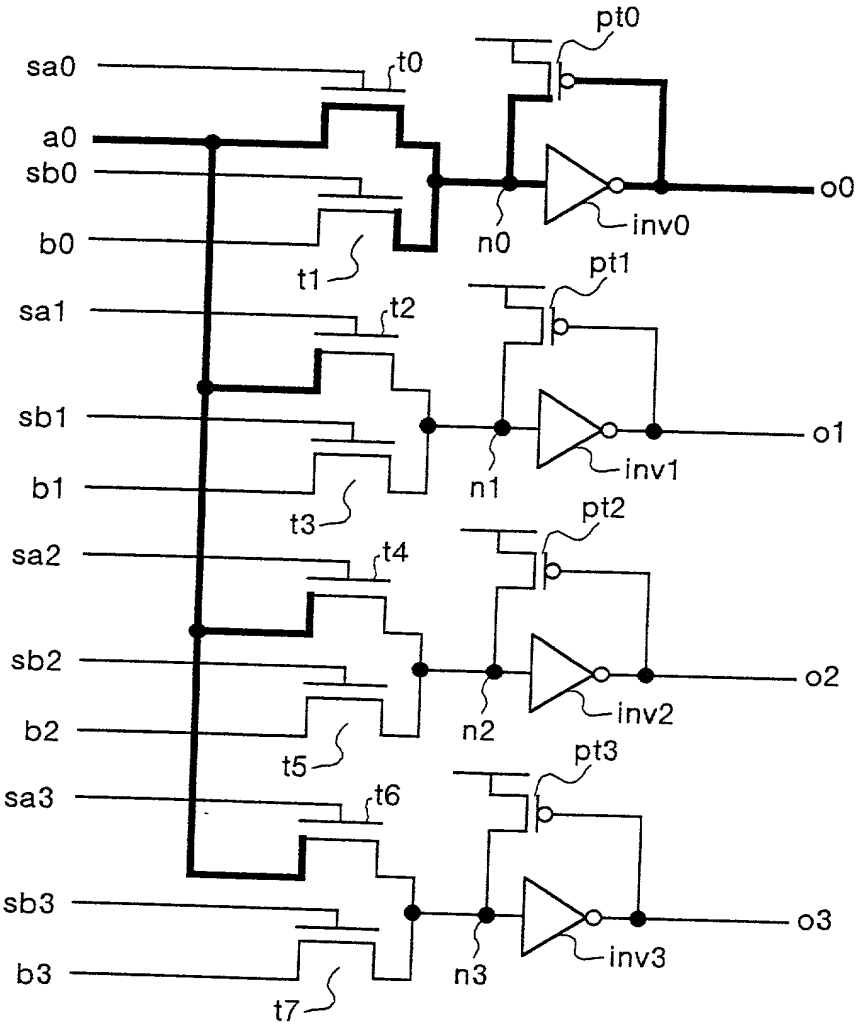

sa0
a0
sb0
b0
sa1
sb1
b1
sa2
sb2
b2
sa3
sb3
b3
t0
t1
t2
t3
t4
t5
t6
t7
pt0
pt1
pt2
pt3
n0
n1
n2
n3
inv0
inv1
inv2
inv3
o0
o1
o2
o3

FIG.8

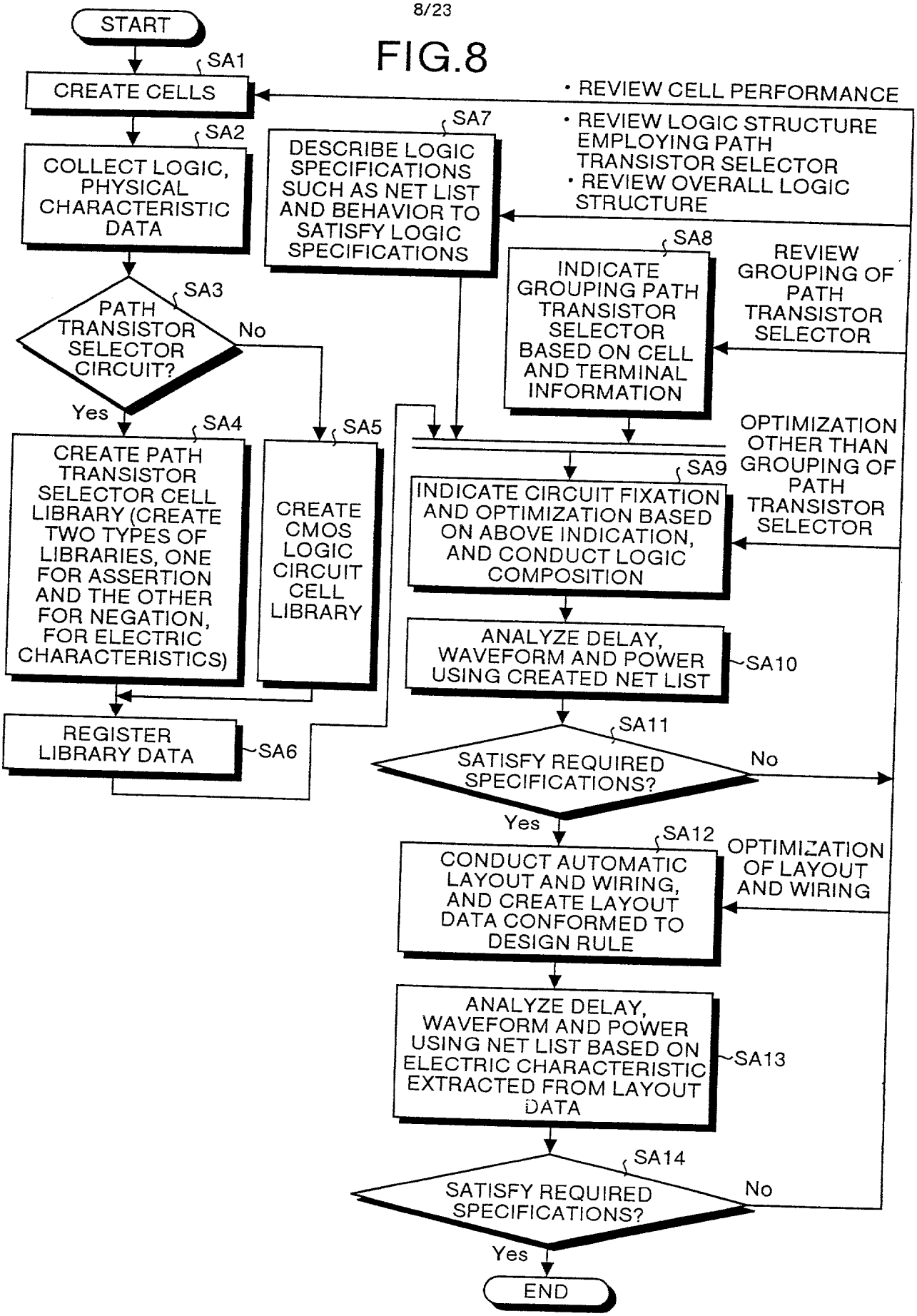

START
SA1
CREATE CELLS
SA2
COLLECT LOGIC, PHYSICAL CHARACTERISTIC DATA
SA3
PATH TRANSISTOR SELECTOR CIRCUIT?
No
Yes
SA4
CREATE PATH TRANSISTOR SELECTOR CELL LIBRARY (CREATE TWO TYPES OF LIBRARIES, ONE FOR ASSERTION AND THE OTHER FOR NEGATION, FOR ELECTRIC CHARACTERISTICS)
SA5
CREATE CMOS LOGIC CIRCUIT CELL LIBRARY
REGISTER LIBRARY DATA
SA6
SA7
DESCRIBE LOGIC SPECIFICATIONS SUCH AS NET LIST AND BEHAVIOR TO SATISFY LOGIC SPECIFICATIONS
• REVIEW CELL PERFORMANCE
• REVIEW LOGIC STRUCTURE EMPLOYING PATH TRANSISTOR SELECTOR
• REVIEW OVERALL LOGIC STRUCTURE
SA8
INDICATE GROUPING PATH TRANSISTOR SELECTOR BASED ON CELL AND TERMINAL INFORMATION
REVIEW GROUPING OF PATH TRANSISTOR SELECTOR
OPTIMIZATION OTHER THAN GROUPING OF PATH TRANSISTOR SELECTOR
SA9
INDICATE CIRCUIT FIXATION AND OPTIMIZATION BASED ON ABOVE INDICATION, AND CONDUCT LOGIC COMPOSITION
ANALYZE DELAY, WAVEFORM AND POWER USING CREATED NET LIST
SA10
SA11
SATISFY REQUIRED SPECIFICATIONS?
No
Yes
SA12
CONDUCT AUTOMATIC LAYOUT AND WIRING, AND CREATE LAYOUT DATA CONFORMED TO DESIGN RULE
OPTIMIZATION OF LAYOUT AND WIRING
ANALYZE DELAY, WAVEFORM AND POWER USING NET LIST BASED ON ELECTRIC CHARACTERISTIC EXTRACTED FROM LAYOUT DATA
SA13
SA14
SATISFY REQUIRED SPECIFICATIONS?
No
Yes
END

FIG.9

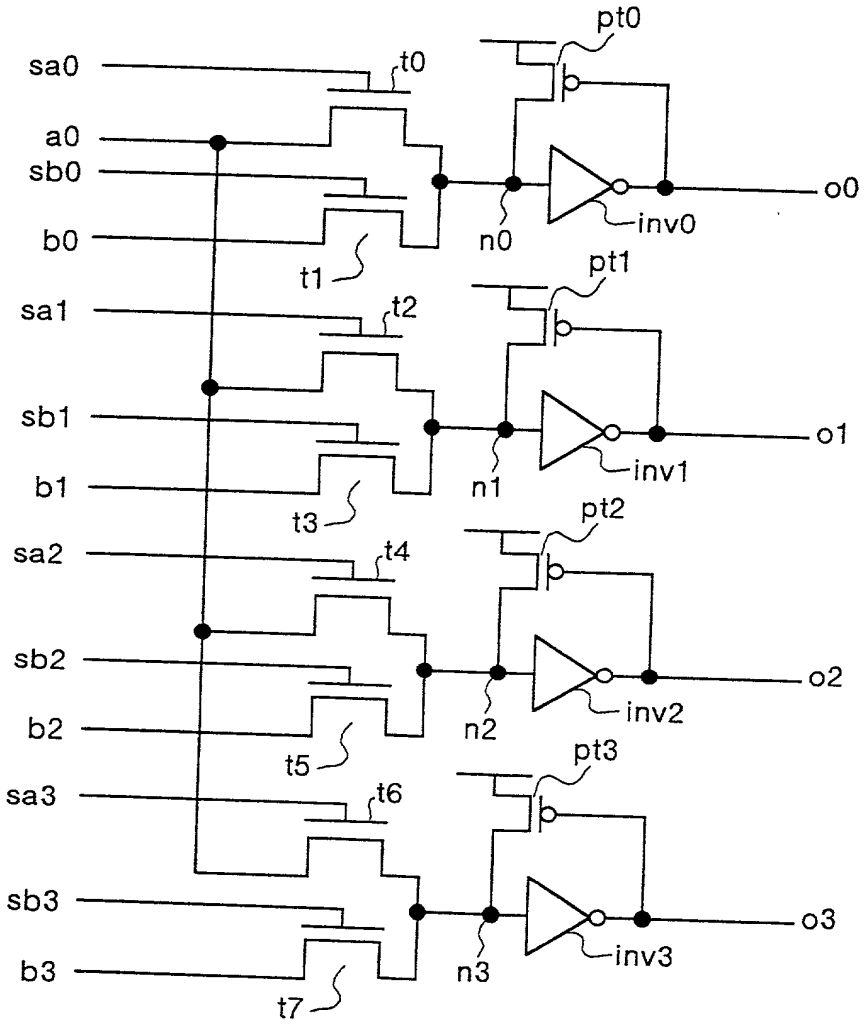

sa0
a0
sb0
b0
sa1
sb1
b1
sa2
sb2
b2
sa3
sb3
b3
t0
t1
t2
t3
t4
t5
t6
t7
pt0
pt1
pt2
pt3
n0
n1
n2
n3
inv0
inv1
inv2
inv3
o0
o1
o2
o3

FIG.10

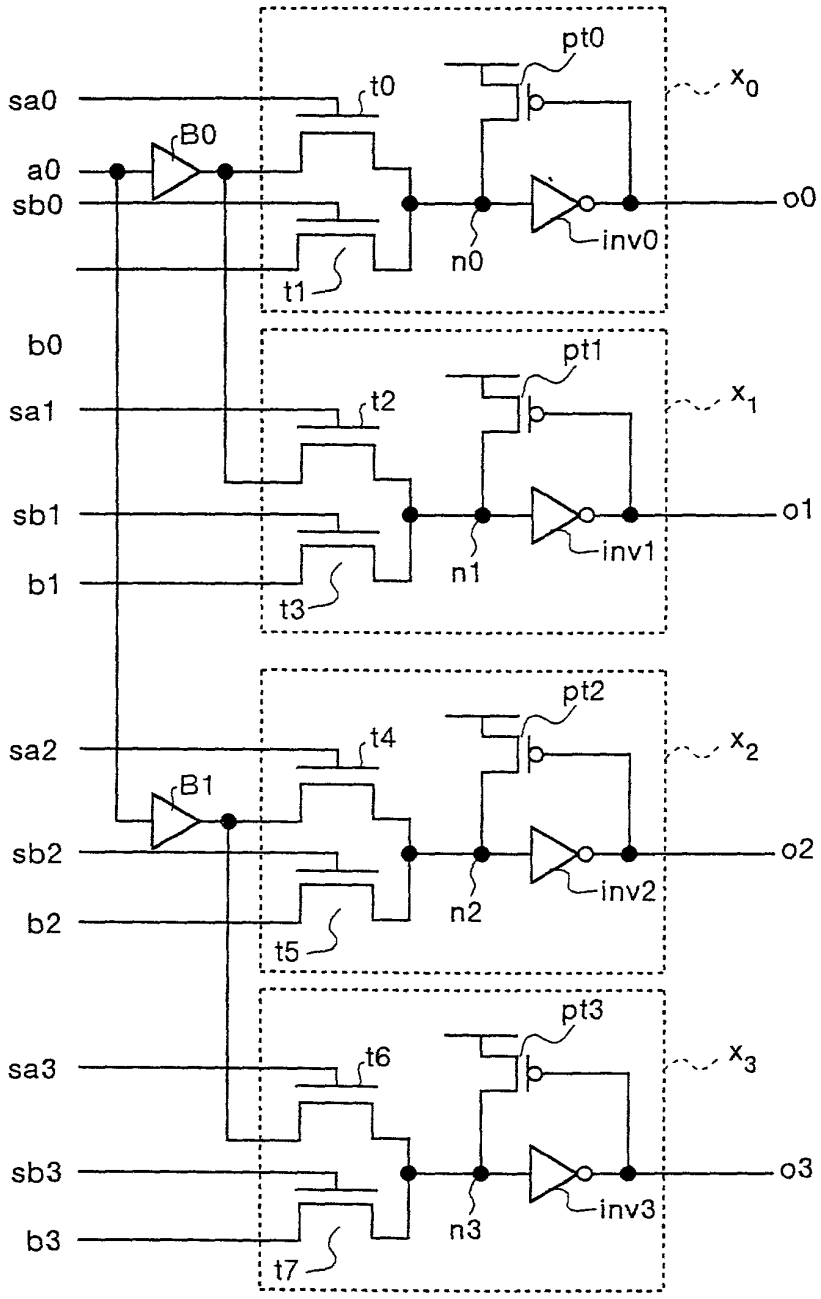

sa0
a0
sb0
B0
t0
t1
pt0
x0
n0
inv0
o0
b0
sa1
sb1
b1
t2
t3
pt1
x1
n1
inv1
o1
sa2
sb2
b2
B1
t4
t5
pt2
x2
n2
inv2
o2
sa3
sb3
b3
t6
t7
pt3
x3
n3
inv3
o3

FIG.11A

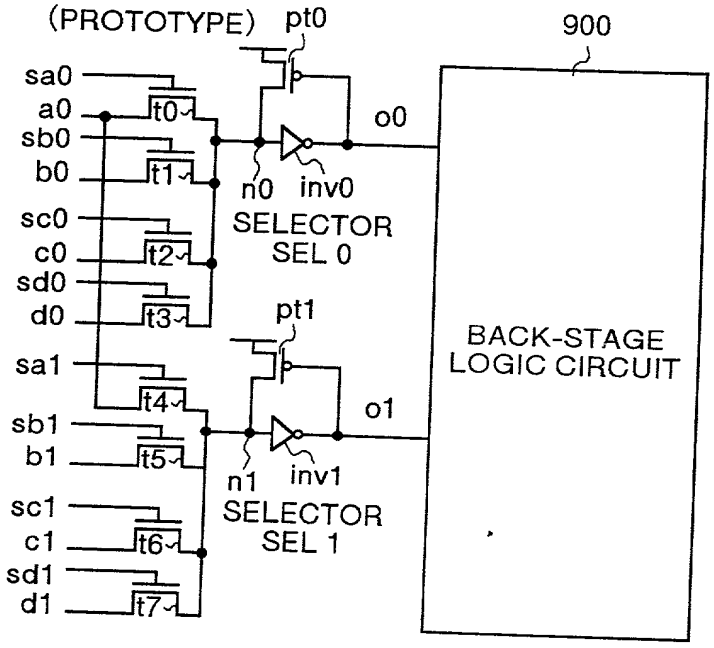


FIG.11B

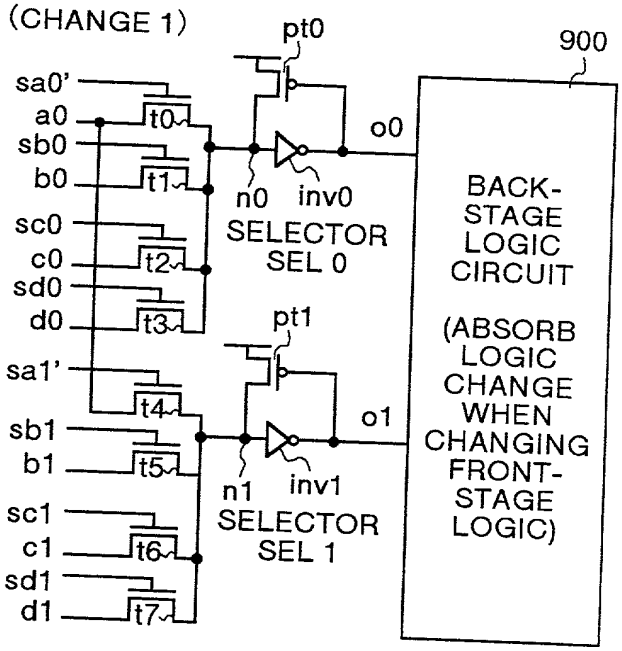


FIG.11C

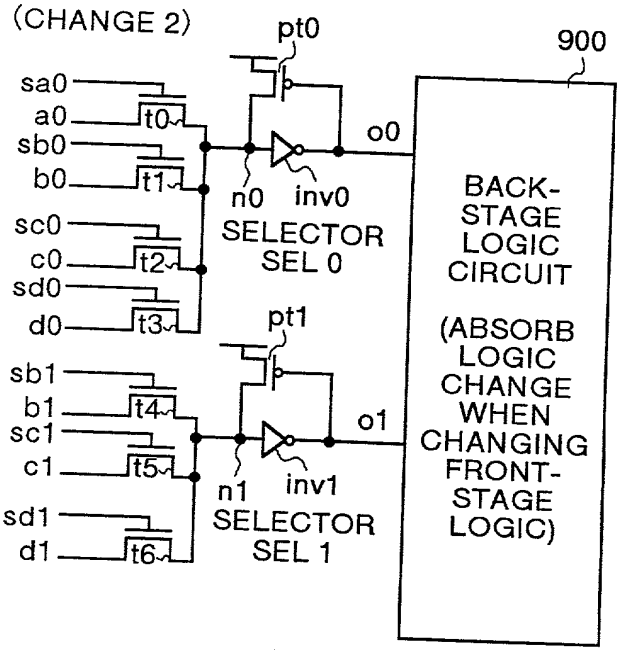


FIG.12A

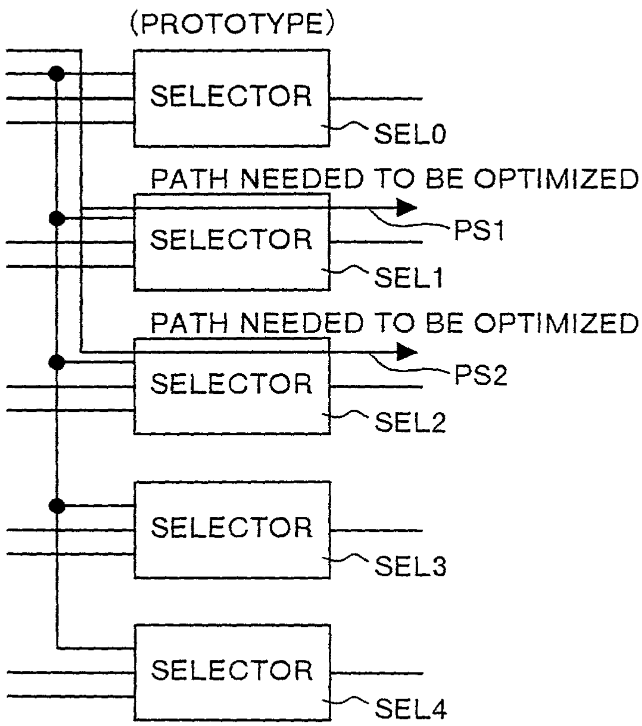


FIG.12B

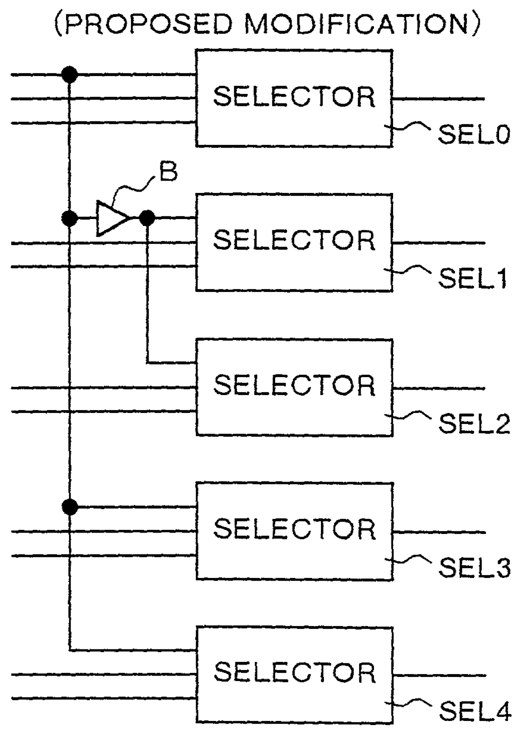


FIG.13A

(PROTOTYPE)

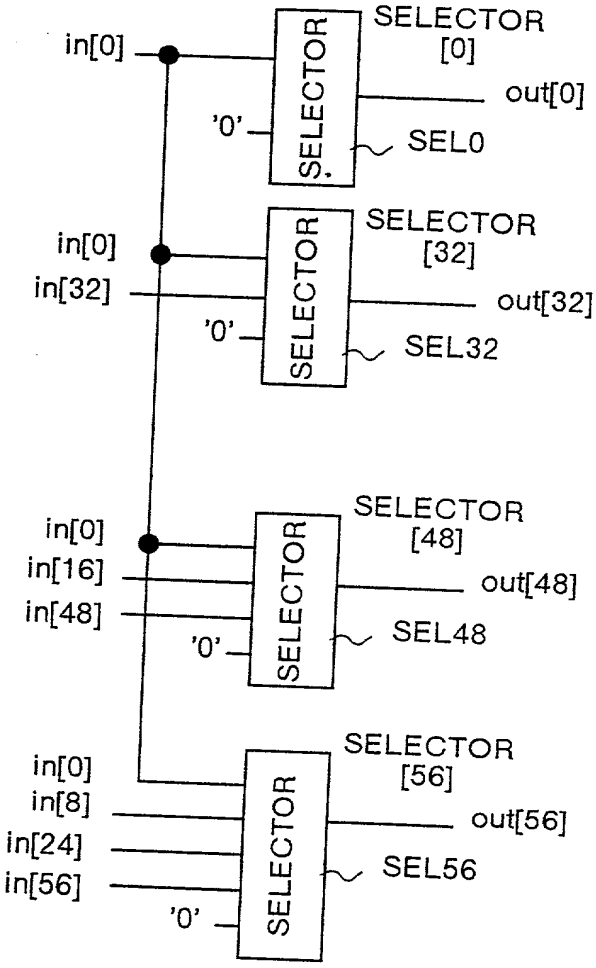


FIG.13B

(PROPOSED MODIFICATION)

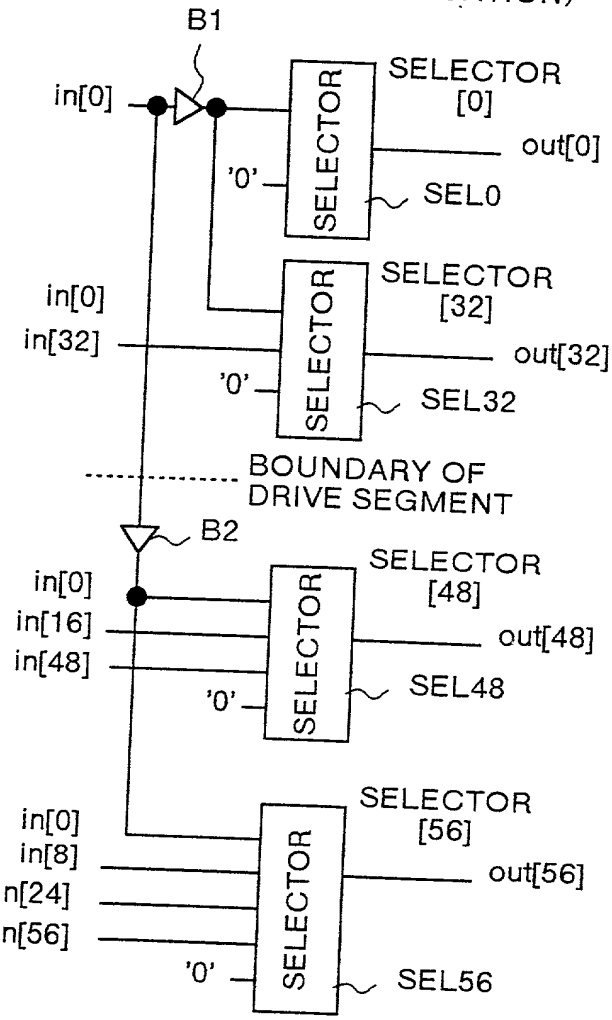


FIG.14

	OUTPUT DATA PATTERN G							
	[0:7]	[8:15]	[16:23]	[24:31]	[32:39]	[40:47]	[48:55]	[56:63]
CONTROL PATTERN 1	all'0'	all'0'	all'0'	all'0'	all'0'	all'0'	all'0'	byte0
CONTROL PATTERN 2	all'0'	all'0'	all'0'	all'0'	all'0'	all'0'	byte0	byte1
CONTROL PATTERN 3	all'0'	all'0'	all'0'	all'0'	byte0	byte1	byte2	byte3
CONTROL PATTERN 4	byte0	byte1	byte2	byte3	byte0	byte1	byte2	byte3
CONTROL PATTERN 5	byte0	byte1	byte2	byte3	byte4	byte5	byte6	byte7

FIG.15

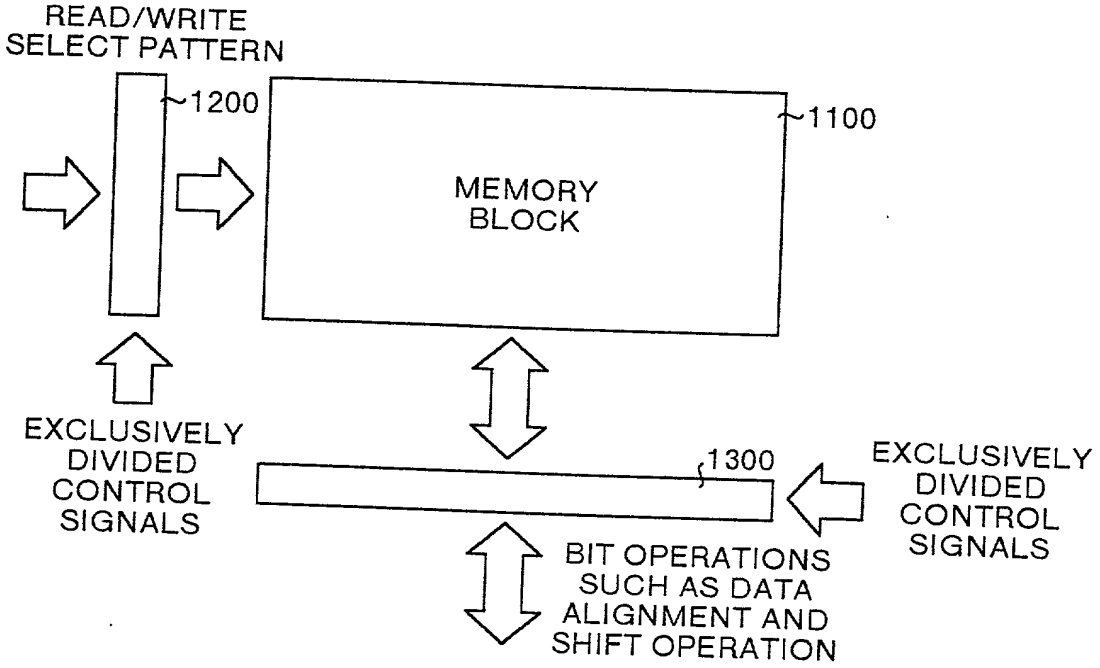


FIG.16

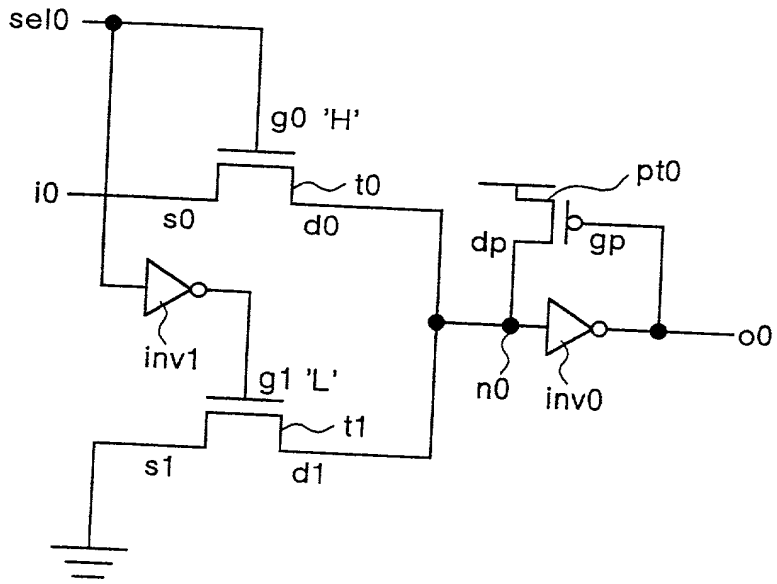

sel0
g0 'H'
i0
t0
pt0
s0
d0
dp
gp
inv1
o0
g1 'L'
n0
inv0
t1
s1
d1

FIG.17

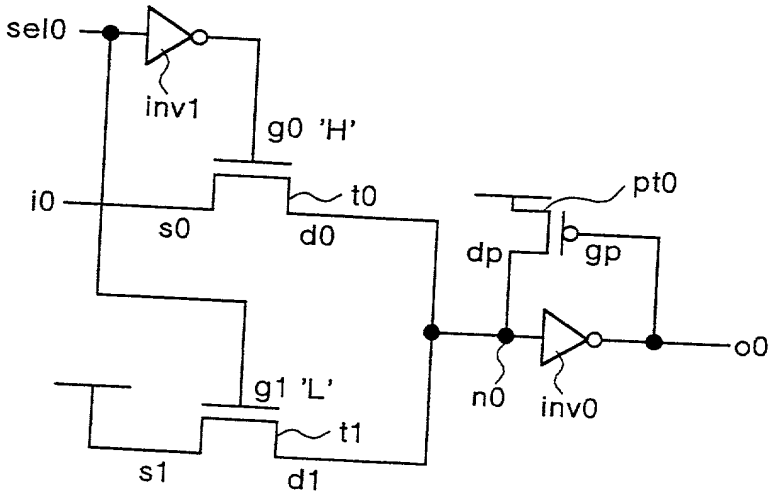

sel0
inv1
g0 'H'
i0
t0
pt0
s0
d0
dp
gp
o0
g1 'L'
n0
inv0
t1
s1
d1

FIG.18

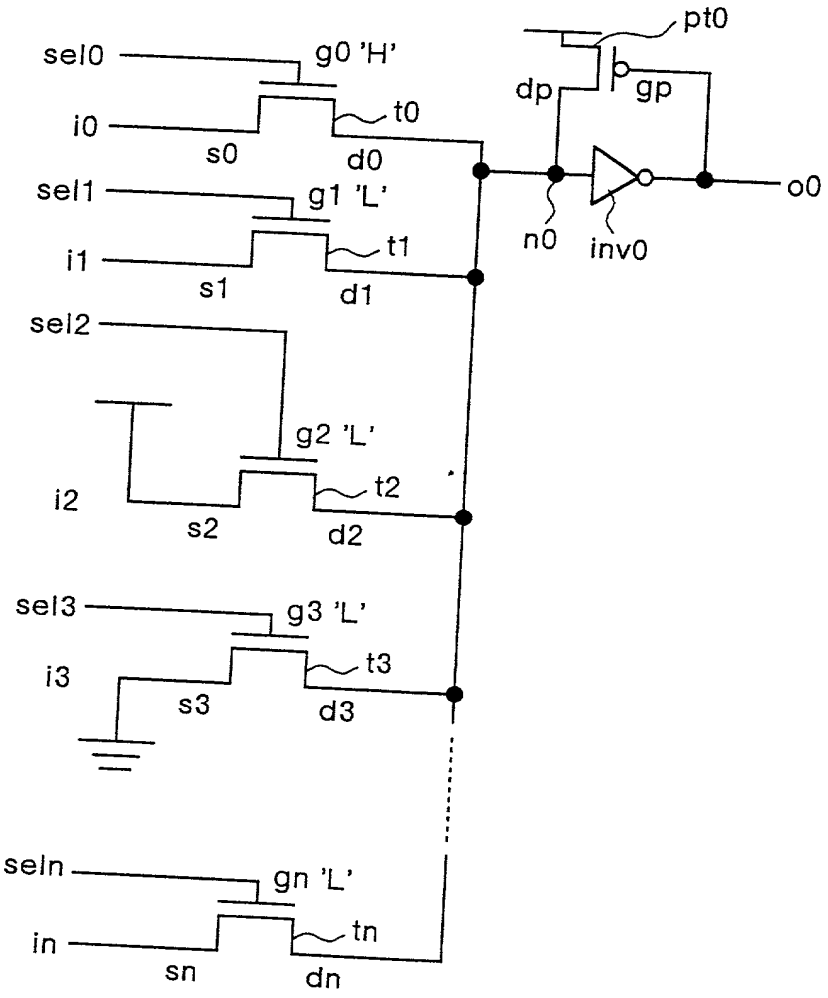

sel0
g0 'H'
i0
t0
s0
d0
sel1
g1 'L'
i1
t1
s1
d1
sel2
g2 'L'
i2
t2
s2
d2
sel3
g3 'L'
i3
t3
s3
d3
seln
gn 'L'
in
tn
sn
dn
pt0
dp
gp
o0
n0
inv0

FIG.19

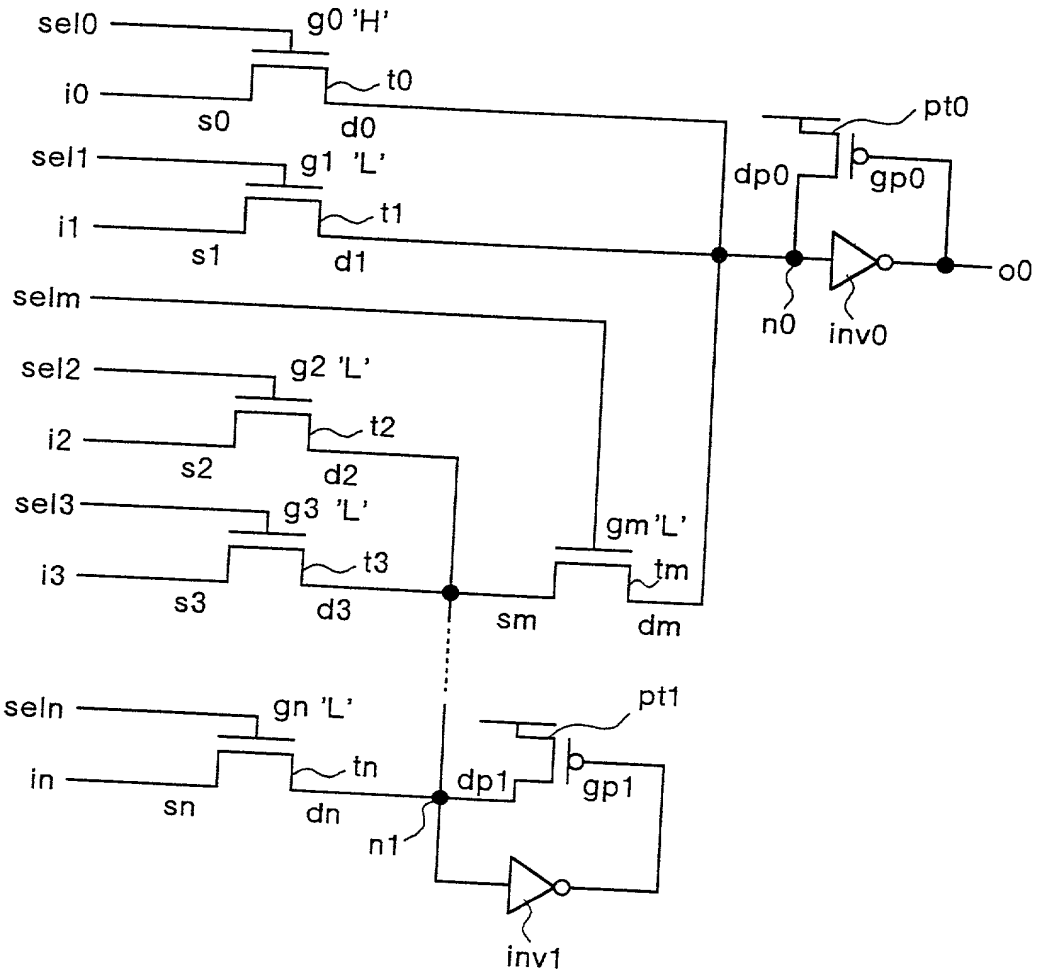

sel0
g0 'H'
i0
t0
s0
d0
pt0
dp0
gp0
sel1
g1 'L'
i1
t1
s1
d1
o0
selm
n0
inv0
sel2
g2 'L'
i2
t2
s2
d2
sel3
g3 'L'
gm 'L'
i3
t3
tm
s3
d3
sm
dm
seln
gn 'L'
pt1
in
tn
dp1
gp1
sn
dn
n1
inv1

FIG.20

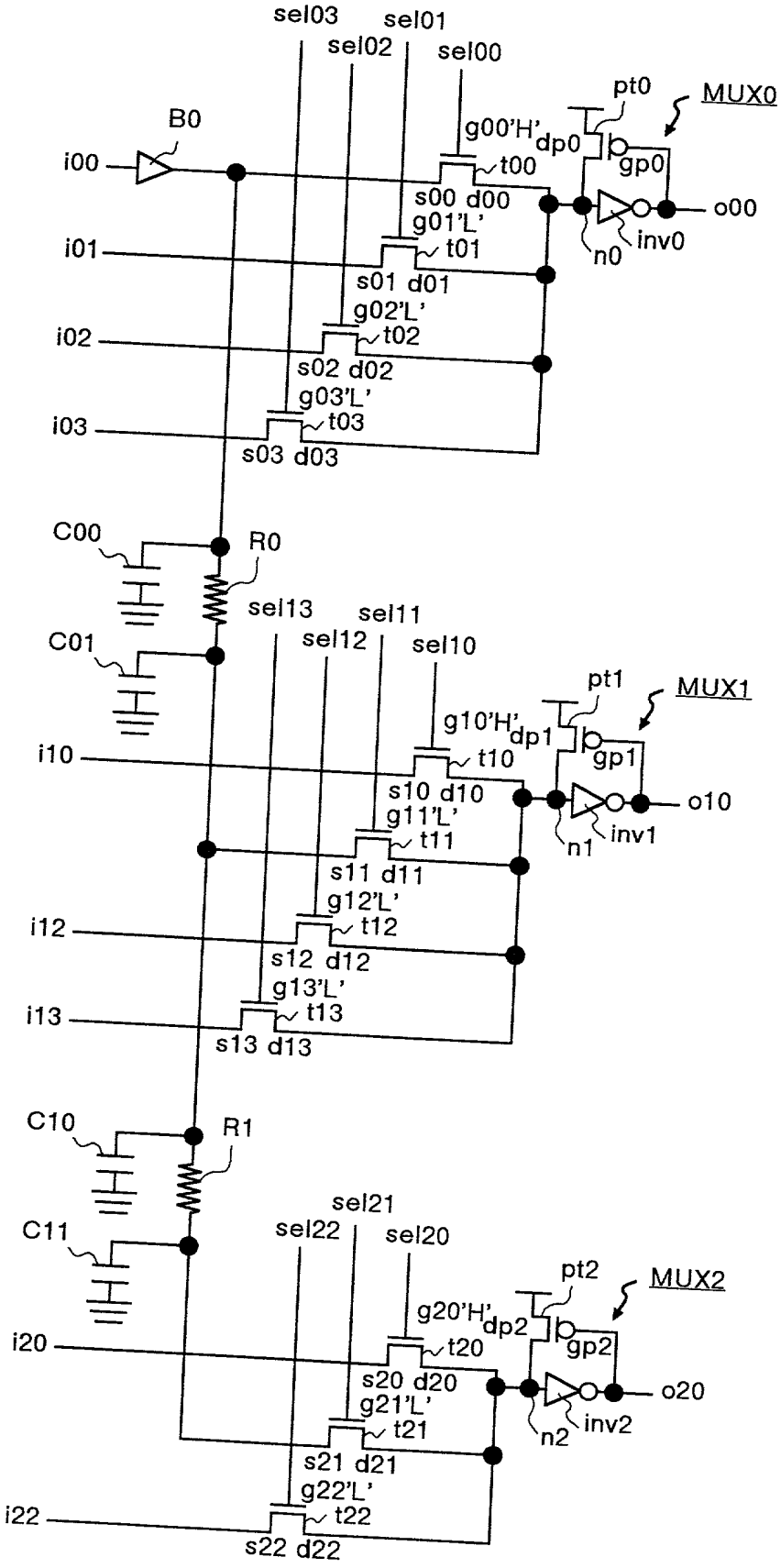

sel03
sel01
sel02
sel00
pt0
MUX0
B0
g00'H'
dp0
gp0
i00
t00
s00 d00
g01'L'
o00
i01
t01
n0
inv0
s01 d01
g02'L'
i02
t02
s02 d02
g03'L'
i03
t03
s03 d03
C00
R0
sel13
sel11
sel12
sel10
C01
pt1
MUX1
g10'H'
dp1
gp1
i10
t10
s10 d10
g11'L'
o10
t11
n1
inv1
s11 d11
g12'L'
i12
t12
s12 d12
g13'L'
i13
t13
s13 d13
C10
R1
sel21
sel22
sel20
C11
pt2
MUX2
g20'H'
dp2
gp2
i20
t20
s20 d20
g21'L'
o20
t21
n2
inv2
s21 d21
g22'L'
i22
t22
s22 d22

FIG.21

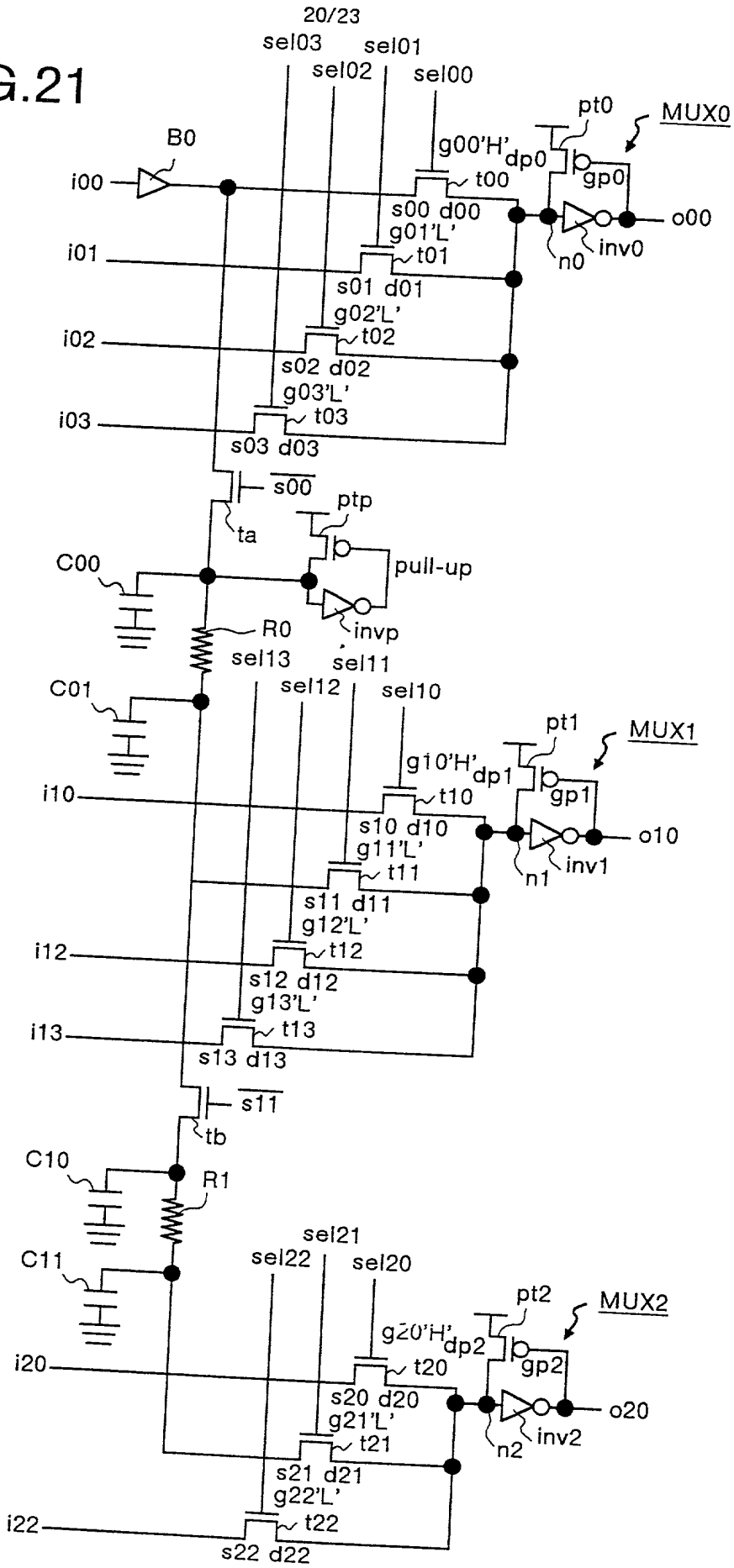

sel03
sel02
sel01
sel00
B0
i00
g00'H'
t00
s00 d00
pt0
MUX0
dp0
gp0
o00
g01'L'
i01
t01
s01 d01
n0
inv0
g02'L'
i02
t02
s02 d02
g03'L'
i03
t03
s03 d03
s00
ptp
ta
C00
pull-up
R0
invp
sel13
sel11
C01
sel12
sel10
pt1
MUX1
g10'H'
dp1
gp1
i10
t10
s10 d10
o10
g11'L'
t11
n1
inv1
s11 d11
g12'L'
i12
t12
s12 d12
g13'L'
i13
t13
s13 d13
s11
tb
C10
R1
sel21
C11
sel22
sel20
pt2
MUX2
g20'H'
dp2
gp2
i20
t20
s20 d20
o20
g21'L'
t21
n2
inv2
s21 d21
g22'L'
i22
t22
s22 d22

FIG.22

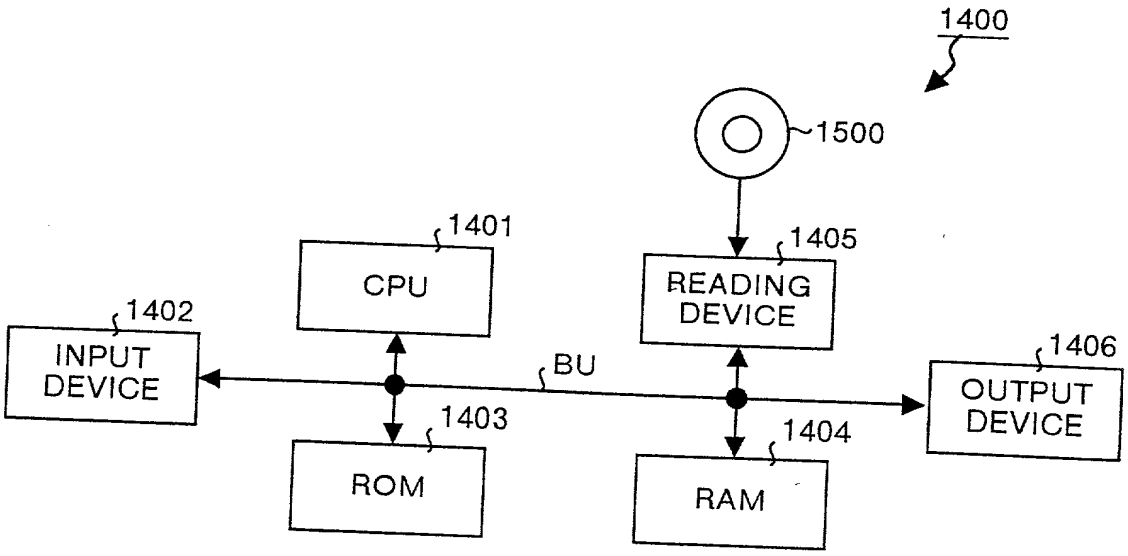

1400
1500
1401
CPU
1405
READING DEVICE
1402
INPUT DEVICE
BU
1406
OUTPUT DEVICE
1403
ROM
1404
RAM

FIG.23A

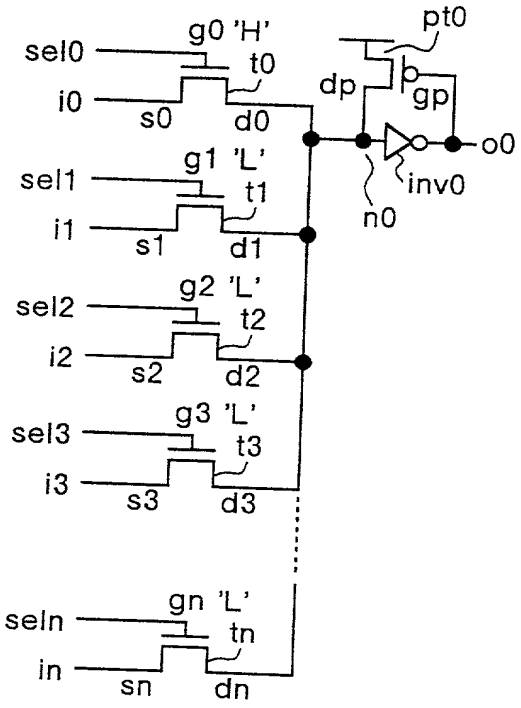


FIG.23B

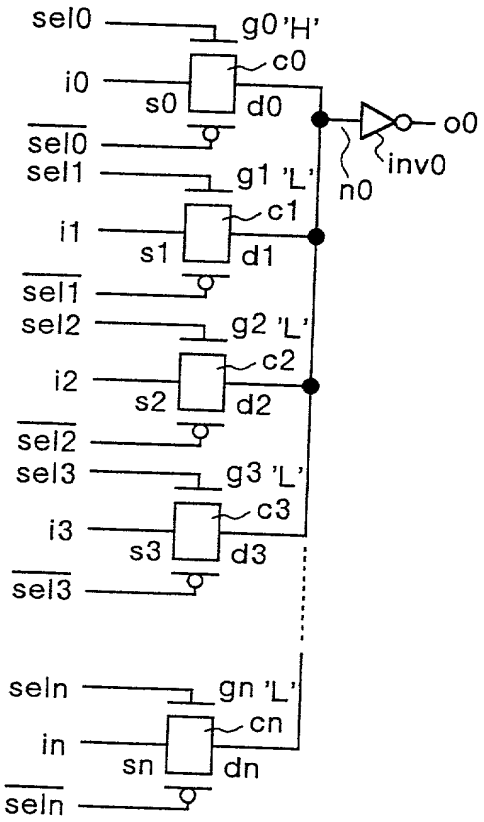
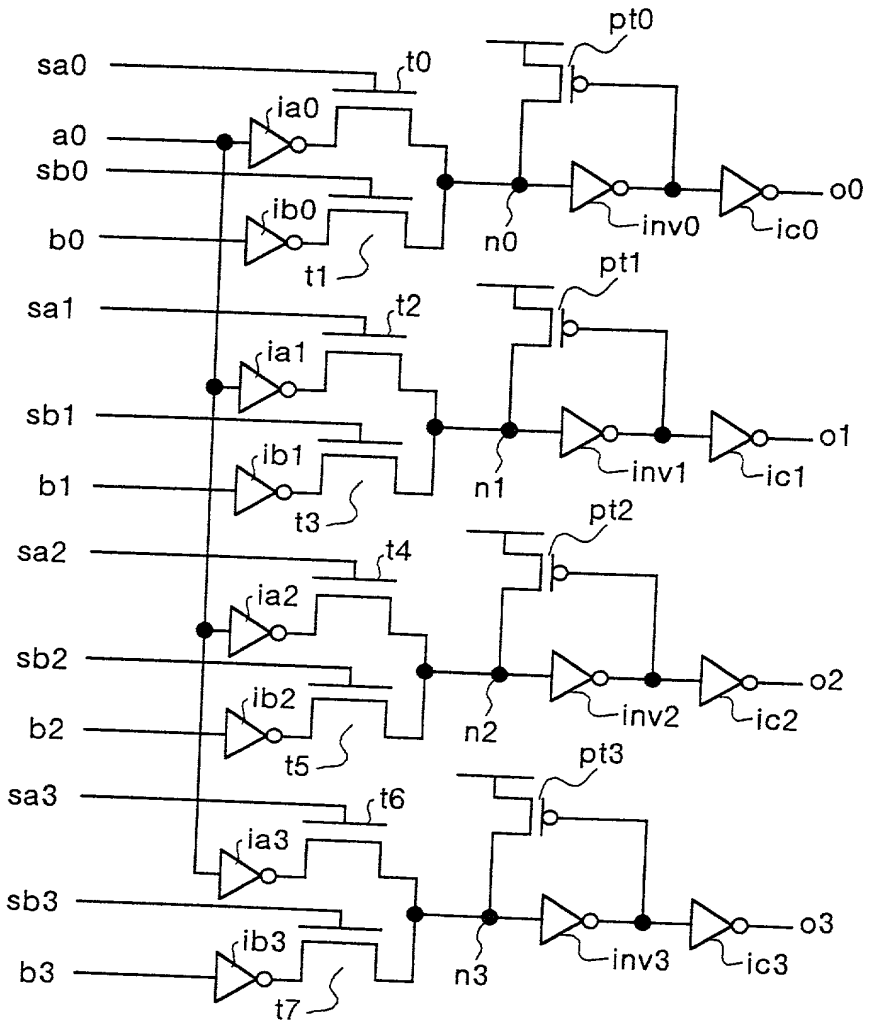


FIG.24


sa0
a0
sb0
b0
sa1
sb1
b1
sa2
sb2
b2
sa3
sb3
b3
t0
t1
t2
t3
t4
t5
t6
t7
ia0
ib0
ia1
ib1
ia2
ib2
ia3
ib3
pt0
pt1
pt2
pt3
n0
n1
n2
n3
inv0
inv1
inv2
inv3
ic0
ic1
ic2
ic3
o0
o1
o2
o3